

# **X-HDL Change Log**

For X-HDL 4.0.34

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July 28, 2008

### **July 28, 2008: X-HDL 4.0.34**

#### **Verilog Translator**

- Added option to translate all parameters to VHDL constants. This helps prevent the problem of one parameter dependent on the value of another parameter.
- Fixed -delay0 option processing.
- Fixed clock identification in always blocks
- Fixed post-processing

#### **VHDL Translator**

- Fixed post-processing
- Fixed formation of a wire assign with a delay
- Fixed syntax of nested generates
- Fixed handling of timescales and scaling of delay values

### **June 23, 2008: X-HDL 4.0.33**

#### **Verilog Translator**

- Fixed sizing of wire with a delay specification in the declaration.
- Fixed translation of wire assignment delays
- Changed translation of wire delays from TRANSPORT to INERTIAL
- Added support for a clk-as-data signal when the signal is referenced outside of an if control clause.

#### **License Manager**

- Fixed loading of license files upon invocation.

### **May 19, 2008: X-HDL 4.0.32**

#### **Verilog Translator**

- Fixed handling of quotes within comments in the Verilog pre-processor

#### **VHDL Translator**

- Fixed translation of instance port names which were the same as signals within the parent component.
- Fixed precedence of unary NOT operator
- Fixed size computation of integer range 0 to 1023 (or any power-of-2 minus 1)
- Fixed translation of (others => ...) within a With-Select clause
- Fixed translation of B'range where B is an array

### **May 12, 2008: X-HDL 4.0.31**

#### **Miscellaneous**

- Updated 3<sup>rd</sup> party libraries

### **Apr. 28, 2008: X-HDL 4.0.30**

#### **Verilog Translator**

- Fixed crash due to nested generates
- Removed incorrect semi-colon following a generic map clause in a component instantiation

## X-HDL Change Log

### **VHDL Translator**

- Fixed processing of VHDL records contained within a package

### **License Manager**

- Corrected server so that it runs as a service under Windows.

### **Known Problems**

- VHDL record elements with a constraint (i.e. BusA.address(3 downto 0)) will generate a bogus missing subprogram message and will incorrectly translate the item with a parenthetical range.

### **Mar. 10, 2008: X-HDL 4.0.29**

#### **Verilog Translator**

- Fixed translation of nested If-statements within a combinational always block

### **Feb. 25, 2008: X-HDL 4.0.28**

#### **Verilog Translator**

- Fixed translation of defparams
- Fixed type-casting of generic overloads

#### **Documentation**

- Corrected format of the custom translation file definitions. They need to be terminated with a semi-colon.

### **Feb. 18, 2008: X-HDL 4.0.27**

#### **Verilog Translator**

- Fixed handling of sensitivity list containing both level- and edge-sensitive elements
- Reverted translation of a select within a initial block to a function call rather than a concurrent assign.

#### **VHDL Translator**

- Fixed handling of a for-loop which caused an application crash

### **Feb. 4, 2008: X-HDL 4.0.26**

#### **Verilog Translator**

- Fixed divide-by-zero problem caused by a denominator within parentheses
- Fixed incorrect type change in select control
- Replaced select\_expr function with intermediate signal
- Changed translation method of LHS concatenation
- Fixed translation of integer parameter used to specify time delays

#### **VHDL Translator**

- Fixed divide-by-zero problem in exponentiation computation

### **Jan. 14, 2008: X-HDL 4.0.25**

#### **Verilog Translator**

## X-HDL Change Log

- Fixed translation of assignment delays
- Added select\_expr function for bit, std\_logic and std\_ulogic parameters.

### **Dec. 11, 2007: X-HDL 4.0.24**

#### **Verilog Translator**

- Fixed determination of array size
- Fixed infinite loop caused by parentheses matching logic

### **Dec. 4, 2007: X-HDL 4.0.23**

#### **Verilog Translator**

- Fixed translation of sequential select expression
- Added option -std2comb which converts standard Verilog gate instances (and, or, not, etc.) to combinational logic.
- Fixed translation of Verilog asserts.

### **Nov. 19, 2007: X-HDL 4.0.22**

#### **VHDL Translator**

- Fixed problem with 'Constants to `defines' option causing incorrect module I/O formatting
- Fixed processing of 'others => ...' where the actual is not '0' or '1'
- Fixed sizing of integers specified by a range
- Fixed translation of 'don't cares' in binary constants
- Fixed translation of unconstrained arrays
- Fixed translation of multi-dimensional arrays

### **Oct. 22, 2007: X-HDL 4.0.21**

#### **VHDL Translator**

- Fixed processing of a declaration that caused application to crash
- Fixed translation of a constant initialized with others =>
- Fixed formatting of if-generate

### **Sep. 12, 2007: X-HDL 4.0.19**

#### **Verilog Translator**

- Removed incorrect parenthesis on case control clause
- Created intermediate signal for case control clause that is an expression
- Corrected translation of a repeated concatenation (i.e. {5{1'b1}})

#### **VHDL Translator**

- Corrected creation of local integer for for-loop iterators

### **May 21, 2007: X-HDL 4.0.18**

#### **Verilog Translator**

## X-HDL Change Log

- Implemented support for Verilog 2001 localparam type
- Removed VHDL string constraint when translating Verilog strings
- Implemented support for sensitivity list globbing
- Corrected translation of sized input re-declared as a sized wire

### **May 7, 2007: X-HDL 4.0.17**

#### **Verilog Translator**

- Corrected mismatched size handling of the operands of binary operators
- Changed translation of the right operand of << and >> to type integer

#### **License Manager**

- Added support for the XLMPORT environment variable to allow users to select the TCP port
- Added support for the XLMOFFSET environment variable to allow users to specify a time skew between the server and client machines.
- Enhanced detection of already running server.

#### **Documentation**

- Added information regarding the XLMPORT and XLMIOFFSET environment variables.

### **Apr. 23, 2007: X-HDL 4.0.16**

#### **Verilog Translator**

- Added support for ANSI –style parameter declarations.
- Added support for custom translation of built-in type-cast functions. and operators
- Added support for string parameters
- Fixed type-casting and sizing of overridden parameter values

#### **VHDL Translator**

- Added support for custom translation of operators
- Fixed declaration of local variables in generate blocks
- Fixed identification of clock expression in process embedded in a block or generate
- Corrected processing of expressions containing capitalized identifiers

### **Apr. 2, 2007: X-HDL 4.0.15**

#### **Verilog Translator**

- Added user-defined output suffix used for X-HDL generated signals for outputs which are referenced.
- Fixed recognition of expressions in port maps

#### **VHDL Translator**

- Fixed handling of if-elsif-else blocks which contained no statements

### **Mar. 21, 2007: X-HDL 4.0.14**

#### **Verilog Translator**

- Created intermediate signals for outputs which are referenced
- Fixed signal names which begin and/or end with an underscore
- Fixed handling of comment placement in files which contain multiple component definitions

### **Mar. 19, 2007: X-HDL 4.0.13**

#### **Verilog Translator**

- Fixed operation of –preserve output option on the Windows platform

#### **VHDL Translator**

- Fixed operation of –preserve output option on the Windows platform

#### **Documentation**

- Corrected reference to XLMSERVER to XLMSERVERS

### **Feb. 26, 2007: X-HDL 4.0.12**

#### **Verilog Translator**

- Fixed operation of –preserve and –single output options

#### **VHDL Translator**

- Fixed operation of –preserve and –single output options
- Fixed hierarchical translation
- Fixed determination of target sizes which affected assignment from ‘others’ clause

### **Feb. 21, 2007: X-HDL 4.0.11**

#### **Verilog Translator**

- Changed method of generation of component declarations to facilitate easier insertion in architecture blocks.

#### **VHDL Translator**

- Fixed identification of a clock expression which contains extra parenthesis sets
- Fixed translation of buffer port

### **Feb. 20, 2007: X-HDL 4.0.10**

#### **Verilog Translator**

- Fixed translation of multiple modules contained within a single file
- Fixed instantiated component name when component name is a VHDL keyword
- Fixed generation of component declarations

#### **VHDL Translator**

- Fixed handling of enumerated type defined within a package. In this case, the type was not being prepended to the enumerated value

### **Feb. 13, 2007: X-HDL 4.0.9**

#### **General**

- Really fixed crash in the command-line version of X-HDL running under windows.

#### **Verilog Translator**

- Fixed translation of unknowns and tristates within constants

## X-HDL Change Log

- Added support for the '?' character in casex statements

### License Manager

- Fixed determination of license end date when running under Windows in non-English environment. This caused incorrect rejection of the license

### **Feb. 5, 2007: X-HDL 4.0.8**

#### General

- Fixed crash in the command-line version of X-HDL running under windows. Problem stemmed from an out-of-date object file in the compilation.

#### Verilog Translator

- Fixed handling of `ifdef directive nested within a `else directive
- Added support for `undef and `ifndef directives
- Fixed handling of implicitly declared wires

### **Jan. 15, 2007: X-HDL 4.0.7**

#### Verilog Translator

- Fixed critical bug in processor affecting `define replacements and ansi-port pre-processing

### **Jan. 10, 2007: X-HDL 4.0.6**

#### VHDL Translator

- Fixed critical bug causing infinite recursion when processing enumerated types

### **Jan. 8, 2007: X-HDL 4.0.5**

#### Verilog Translator

- Fixed incorrect insertion of intermediate wires on simple port connects
- Fixed type-casting from boolean to std\_logic/std\_ulogic/bit

#### VHDL Translator

- Fixed infinite recursion problem due to arrays within a function. Note that the arrays are not translated properly, yet.
- Fixed inclusion of one package into another
- Fixed translation of entity/architectures which are in separate files. Note that files still need to be translated together – i.e. you cannot translate the entity and then translate the architecture multiple times.

#### Packages

- Added boolean to std\_logic\_vector/std\_ulogic\_vector/bit\_vector conversion functions

### **Dec. 19, 2006: X-HDL 4.0.4**

#### Verilog Translator

## X-HDL Change Log

- Fixed custom translation support for tasks and functions
- Fixed translation of numerical port connect
- Fixed handling of for-loops
- Fixed expression evaluation order when translating the results of binary operations to boolean
- Fixed translation of the special case of a Verilog select to a wire assign.
- Added auto-inclusion of X-HDL packages when referenced in the translated code.

### **VHDL Translator**

- Added support for records declared within a package

### **Packages**

- Added std\_logic/std\_ulogic/bit to integer conversion functions

## **Dec. 11, 2006: X-HDL 4.0.3**

### **General**

- Added ability to wait for a license to become available. In command-line mode, the `-queue` option forces a wait for license. In GUI mode, the application waits automatically, which can be canceled by the user.

### **Verilog Translator**

- Added `-param2int` command-line option which forces translation of parameters into integer constants regardless of parameter size.
- Fixed type-casting of parameter init values.
- Added `-package` command-line option which aids in translating ``include-d` files into VHDL packages.
- Added support for Verilog-2001 register initialization.
- Fixed pre-processing of nested ``else` and ``endif` directives
- Added support for translation of `$time`.
- Fixed operation of `-define` command-line option.
- Modified code generation to suppress unnecessary multiple blank lines
- Fixed insertion of multiple local subprograms into a process declaration section.
- Removed incorrect "return" clause from procedure declarations.
- Fixed operation of the `-incpath` command-line option

### **VHDL Translator**

- Added warning for array return types in functions
- Fixed function return type of bounded integer
- Modified code generation to suppress unnecessary multiple blank lines.
- Added support for record expansion in statements and subprogram parameter lists. Note that record types declared in a package are currently not recognized. This will be corrected in the next release.

### **License Manager**

- Fixed date manipulation which failed when locale was not English

### **Documentation**

- Updated figures for GUI changes
- Added documentation on new Verilog `-package` and `-param2int` command-line options
- Added documentation for the new `-queue` command-line option
- Added section for Translation Limitations and Considerations

### **Nov. 27, 2006: X-HDL 4.0.2**

#### **Verilog Translator**

- Fixed crash due to improper storage of if-generate block statements

#### **License Manager**

- Fixed generation of Linux/Unix hostids
- Created additional license refresh states

#### **Documentation**

- Corrected references to License Manager XLMSERVERS environment variable.

### **Nov. 22, 2006: X-HDL 4.0.1a**

#### **License Manager**

- Corrected xlmserver startup from application
- Made xlmserver backwards compatible with X-HDL 4.0.0 server protocol

### **Nov. 20, 2006: X-HDL 4.0.1**

#### **General**

- Enabled hierarchical translation from GUI mode
- Fixed destination directory when -dest is not specified on the command line
- Fixed crash due to source file not found
- Modified license priority (bi-dir/uni-dir) for command-line mode vs. GUI mode.
- Added Help->Server Messages menu to access debug info from license server
- Help->User's Manual now auto-invokes the system .pdf reader
- System upgraded to Qt 4.2 libraries

#### **VHDL Translator**

- Partially implemented translation of VHDL records. **Does not auto-expand references to a record.**
- Modified parser to accept 'end package body;', 'end entity;' and 'end architecture;' syntax

#### **Verilog Translator**

- Fixed crash due to `include file not found
- Corrected array translation
- Corrected parsing of `timescale directive
- Added support for `define directive which spans multiple lines
- When translating a case statement, added missing 'is' keyword to VHDL case
- Added warnings and proper handling of unsupported system tasks and functions

#### **License Manager**

- Fixed case sensitivity of host ID
- Added additional debug message to xlmserver
- Added support for MAC address host ID's on Unix/Linux platform
- Fixed formatting of Unix/Linux host ID derived from internal integer

## X-HDL Change Log

### **Oct. 30, 2006: X-HDL 4.0.0**

- Initial Release